

Appl. No. 10/786,604
Arndt dated September 22, 2005
Reply to Office Action of July 12, 2005

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please amend claims 1 and 7 as follows:

1. (currently amended): An eventpoint chaining apparatus for generalized event detection and action specification in a processing environment comprising:
 - a first processing element having a programmable eventpoint module with an input trigger (InTrig) input ~~and two outputs, the first processing element detecting an occurrence of a first processor event (p-event) one which~~ and producing an OutTrigger (OT) signal ~~and one which produces an EP interrupt signal;~~
 - a second processing element having a programmable eventpoint module with an input trigger (InTrig) input ~~which receives the OT signal from the first processing element and two outputs one which, the second processing element detecting an occurrence of a second p-event and producing an OutTrigger (OT) signal and one which produces, in response to the OT signal received from the first processing element and the detected second p-event, an eventpoint (EP) interrupt signal, the InTrig input of the second processing element connected to the OT output of the first processing element and the InTrig input of the first processing element connected to the OT output of the second processing element; and~~

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a sequence processor interrupt control unit for receiving processing element the EP interrupt signals indicating the occurrence of both the first and second p-events and causing a processor action (p-action) in response to the occurrence of both the first and second p-events.

2. (original): The apparatus of claim 1 wherein each of said eventpoint modules further comprises:

means for detecting a generalized processor event (p-event) comprising a change of state it is desirable to recognize; and

means for implementing a generalized processor action (p-action) in acknowledgement in response to the detection of the generalized p-event.

3. (original): The apparatus of claim 1 wherein the first processing element is a sequence processor.

4. (original): The apparatus of claim 1 wherein the first and second processing elements are array processor elements.

5. (original): The apparatus of claim 1 wherein the first and second processing elements both further comprise a special purpose register (SPR) or registers for the storage of the eventpoint parameters.

6. (original): The apparatus of claim 5 wherein eventpoints are separated into two basic classes, instruction eventpoints and data eventpoints and both classes of eventpoints are stored in the SPR file.

7. (currently amended): An eventpoint chaining apparatus for generalized event detection and action specification in a processing environment comprising:

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a processing element having at least a first and a second programmable eventpoint module, each programmable eventpoint module with having an input trigger (InTrig) input, a first output, and two a second outputs, one which produces an OutTrigger (OT) signal and one which produces an eventpoint (EP) interrupt signal;

the InTrig of the second eventpoint module connected to the OTfirst output of the first eventpoint module and the InTrig of the first eventpoint module connected to the OT output of the second eventpoint module for the purpose of chaining eventpoints within the processing element, the first programmable eventpoint module detecting an occurrence of a first processor event (p-event) and producing an OutTrigger (OT) signal over the first output of the first programmable eventpoint module; and

the second programmable eventpoint module receiving the OT signal over the InTrig input, detecting an occurrence of a second p-event and, in response to the received OT signal and detected second p-event, producing an eventpoint (EP) interrupt signal over the second output to cause a processor action (p-action) in response to the occurrence of both the first and second p-events.

8. (original): The apparatus of claim 7 wherein the processing element is a sequence processor.

9. (original): The apparatus of claim 7 wherein one eventpoint module is for an instruction eventpoint and the other eventpoint module is for a data eventpoint.

10. (original): The apparatus of claim 7 wherein both eventpoint modules are for instruction eventpoints.

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11. (original): The apparatus of claim 7 wherein both eventpoint modules are for data eventpoints.